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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,178	11/26/2003	Shih-Lien L. Lu	INTEL-0034	6618

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EXAMINER	
KIM, DANIEL Y	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,178	LU ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 May 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-25 and 27-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-15,18,20,25,27,28,31 and 33-37* is/are rejected.

7)☒ Claim(s) *16,17,19,21-24,29,30,32 and 38-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2005 and 26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed May 1, 2006 in response to the PTO Office Action mailed January 30, 2006. The applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.

2. In response to the last Office Action, claims 6-9, 11-12, 14-15, 17-19 and 25 have been amended, claims 1-5 and 26 are canceled and claims 27-40 are added. Claims 6-25 and 27-40 remain pending in this application.

3. The rejection of claim 1 under 35 U.S.C. 112 has been withdrawn due to the amendment filed May 1, 2006.

Response to Arguments

4. Applicant's arguments with respect to claims 6-25 and 27-40 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 6-8, 20 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994) and Bhattacharya et al (US Patent No. 7,047,385).

For claim 6, Miller discloses a memory comprising a plurality of systolic memory arrays (systolic memory arrays that grow in size as the number of inputs grow, par. 0035).

Miller fails to disclose the remaining claim limitations.

Bhattacharya, however, helps disclose each array is divided into banks, each of the memory arrays arranged in a pipelined architecture and each of the plurality of memory arrays to support pipeline access to the corresponding banks using a plurality of data pipes (multiple arrays of memory banks, col. 3, lines 35-36; addresses input from an address interface by an address pipeline and data read from memory blocks to a data out interface by a data pipeline, col. 1, lines 51-54).

Miller and Bhattacharya are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include dividing memory arrays into banks and supporting pipelined architecture because this would allow for high-capacity, high-speed external memory wherein data can be read from the memory at the speed of the memory blocks and speed is not decreased by increasing the capacity of the memory (col. 1, lines 55-58), as taught by Bhattacharya.

For claim 7, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

Bhattacharya further helps disclose at least one of the plurality of data pipes is used for a reading operation (data is read from memory blocks supplied to a data out interface of an integrated circuit by a data pipeline, col. 1, lines 53-54).

For claim 8, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

Bhattacharya further helps disclose at least one of the plurality of data pipes is used for a writing operation (a pipeline couples an internal write data bus to the interface, col. 3, lines 44-45).

For claim 20, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

Bhattacharya further helps disclose whenever a bank receives a read address, memory access is initiated (each memory bank in an array can complete a single read or write transaction in one clock cycle; the memory banks are coupled in parallel to internal read and write data buses and an address bus; an interface includes an input interface to receive address, command, and write data and an output interface to output read data, col. 3, lines 24-32).

Claim 35 is rejected using the same rationale as for the rejection of claim 6 above.

7. Claims 9 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385) and Potter (US Patent No. 6,505,269).

For claim 9 the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose the limitations of the current claim.

Potter, however, helps disclose each of the plurality of systolic memory arrays includes at least eight banks (there are preferably eight independent banks of memory available to the processors, col. 7, lines 41-43).

Miller, Bhattacharya and Potter are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include at least eight banks in each array because this arrangement is significant to a streaming mode of operation wherein interleaving occurs between the banks and the arrays (col. 7, lines 43-45), as taught by Potter.

For claim 18, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose the limitations of the current claim.

Potter, however, helps disclose memory operations from different banks having different memory addresses of one of the systolic memory arrays are interleaved (interleaving occurs between banks and arrays of memory, col. 7, line 45).

Miller, Bhattacharya and Potter are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention to allow different memory addresses to be interleaved because this arrangement contributes to a streaming mode of operation (col. 7, lines 43-45), as taught by Potter.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385) and Martin et al (US PGPub No. 20020156995).

For claim 10, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose the limitations of the current claim.

Martin, however, helps disclose a number of pipeline stages used depends upon an access latency of each bank and a desired throughput rate (the optimal number of stages for maximum throughput is determined by the ratio of the cycle period over the forward latency of a pipeline stage, par. 0115).

Miller, Bhattacharya and Martin are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention that a number of pipeline stages used depends upon an access latency of each bank and a desired throughput rate because, when fine pipelines are desirable, the number of pipeline

stages may be changed in order to achieve desired high-throughput and low latency (par. 0096), as taught by Martin.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385) and Tsuruta et al (US PGPub No. 20030037226).

For claim 11, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose the limitations of the current claim.

Tsuruta, however, helps disclose a clock frequency and a data path width for the pipeline architecture is determined (a processor architecture comprising a pipeline, shared by each of the program streams, having N pipeline stages operable at a frequency F, an instruction developing section which develops one instruction into Q parallel instructions, and a first mechanism executing one program stream for every M cycles depending on a required operation performance and selectively executing the Q parallel instructions, par. 0018).

Miller, Bhattacharya and Tsuruta are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention that a clock frequency and data path width for a pipeline may be determined because this would allow for the system to suit a required performance and further reduce power consumption (par. 0018), as taught by Tsuruta.

10. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385) and Zahir et al (US Patent No. 6,052,802).

For claim 12, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose the limitations of the current claim.

Zahir, however, helps disclose a number of pipeline stages relates to a number of clock cycles (a number of computer cycles equal to the number of pipeline stages contained in a computer, col. 1, lines 26-27).

Miller, Bhattacharya and Zahir are analogous art in that they are of the same field of endeavor, that is, a system and method for memory control. It would have been obvious to a person of ordinary skill in the art at the time of the invention to make a number of pipeline stages related to a number of clock cycles because it is common knowledge that a design technique called a pipeline involves the output of one process to serve as input to a second, etc., during which one or more processes occur during a computer clock cycle (col. 1, lines 13-20), as taught by Zahir.

Claim 13 is rejected using the same rationale as for the rejection of claim 12 above.

11. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385) and Witt et al (US Patent No. 5,867,683).

For claim 14, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose the limitations of the current claim.

Witt, however, helps disclose each of the plurality of systolic memory arrays is divided into a horizontal arrangement (stages of a microprocessor pipeline are listed horizontally at the top of timing diagrams, col. 32, lines 32-33).

Miller, Bhattacharya and Witt are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention to divide the pipelined memory array into horizontal and vertical arrangements because this would illustrate the status of selected signals in a microprocessor throughout the multiple stages of the pipeline thereof (col. 32, lines 19-21), as taught by Witt.

For claim 15, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose the limitations of the current claim.

Witt, however, helps disclose each of the plurality of systolic memory arrays is divided into a vertical arrangement (signals which composes timing diagrams are listed vertically at the left of the diagrams, col. 32, lines 33-35).

Miller, Bhattacharya and Witt are analogous art in that they are of the same field of endeavor, that is, a memory device and the control thereof. It would have been obvious to a person of ordinary skill in the art at the time of the invention to divide the pipelined memory array into horizontal and vertical arrangements because this would illustrate the status of selected signals in a microprocessor throughout the multiple stages of the pipeline thereof (col. 32, lines 19-21), as taught by Witt.

12. Claims 25, 28, 34 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385) and Berg et al (US Patent No. 6,732,247).

For claim 25, the combined teachings of Miller and Bhattacharya disclose the invention as per rejection of claim 6 above.

These teachings fail to disclose the limitations of the current claim.

Berg, however, helps disclose a processing system comprising:

a die including a microprocessor (a processor die serving as an addressable on-chip memory, col. 1, line 67; col. 2, line 1);

peripheral equipment coupled to the processing system (the computing system also includes a display, one or more input devices, one or more peripheral devices, col. 3, lines 23-31);

a network interface (computing system with pipelined data banks may include a communication or network interface, col. 3, lines 32-34); and on-die and off-die storage media wherein said storage media is a memory array (a multi-ported pipelined memory

that is located on a processor die serving as an addressable on-chip memory, col. 1, lines 66-67, col. 2, line 1); and

on-die or off-die systolic memory, the systolic memory including:

a plurality of separate systolic memory arrays, each memory array including a plurality of memory banks in a pipelined fashion, the plurality of memory banks of each memory array to share an address line in a pipelined fashion and data lines in a pipelined fashion (Miller: par. 0035; Battacharya: col. 3, lines 35-36; col. 1, lines 51-54).

Claim 28 is rejected using the same rationale as for the rejections of claims 6 and 25 above.

Claim 34 is rejected using the same rationale as for the rejections of claims 6 and 28 above.

Claim 37 is rejected using the same rationale as for the rejections of claims 28 and 35 above.

13. Claims 27, 31, 33 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US PGPub No. 20040100994), Bhattacharya et al (US Patent No. 7,047,385), Berg et al (US Patent No. 6,732,247) and Potter (US Patent No. 6,505,269).

For claim 27, the combined teachings of Miller, Bhattacharya and Berg disclose the invention as per rejection of claim 25 above.

These teachings fail to disclose the limitations of the current claim.

Potter, however, helps to disclose the systolic memory further comprises a plurality of pipeline registers, each register coupled to one of the separate systolic memory arrays (an address mapper implemented as a plurality of hardware registers, wherein a controller selects certains bits from an address to determine the particular bank and array to which a memory access operation is directed, col. 11, lines 5-15).

Miller, Bhattacharya, Berg and Potter are analogous art in that they are of the same field of endeavor, that is, a system and/or method of memory management. It would have been obvious to a person of ordinary skill in the art at the time of the invention to include pipeline registers because this would help a processor in issuing a particular access (read/write) operation to a memory resource at a particular address (col. 10, lines 61-63), as taught by Potter.

Claim 31 is rejected using the same rationale as for the rejections of claims 6 and 27 above.

Claim 33 is rejected using the same rationale as for the rejection of claim 31 above.

Claim 36 is rejected using the same rationale as for the rejections of claims 27 and 35 above.

Allowable Subject Matter

14. The following is a statement of reasons for the indication of allowable subject matter:

For claim 16, no combination of the aforementioned references describe pumping an address with data that is to be written into memory.

For claim 17, no combination of the aforementioned references describe pumping an address once and allowing the address to flow through an address pipe to reach individual banks of one of the systolic memory arrays one cycle at a time.

For claim 19, no combination of the aforementioned references describe peripheral access for one systolic memory array is accomplished from one side of the one systolic memory array.

For claim 21, no combination of the aforementioned references describe access latency for a bank is represented by 2i+L, where i represents the time it takes to allow an address to reach a desired i th bank and L represents the cycles of latency to access the memory.

Claims 22-24 are allowable as being, directly or indirectly, dependent on claim 21 and having additional allowable features therein.

For claim 29, no combination of the aforementioned references describe a read operation from memory is performed by pumping an address once and allowing the address to flow through an address pipe to reach individual banks one cycle at a time.

For claim 30, no combination of the aforementioned references describe access latency for a bank is represented by 2i+L, where I represents the time it takes to allow an address to reach a desired i th bank and L represents the cycles of latency to access the memory.

For claim 32, no combination of the aforementioned references describe each register is coupled to one end of a corresponding one of the systolic memory arrays.

For claim 38, no combination of the aforementioned references describe a read operation is performed by pumping an address and allowing the address to flow through the address line to reach individual banks of one of the plurality of separate systolic memory arrays one cycle at a time.

For claim 39, no combination of the aforementioned references describe access latency for one bank of one of the plurality of separate systolic memory arrays is represented by 2i+L, where I represents time it takes to allow an address to reach a desired i th bank and L represents cycles of latency to access the memory.

For claim 40, no combination of the aforementioned references describe peripheral access for one systolic memory array is accomplished from one side of the one systolic memory array.

Citation of Pertinent Prior Art

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Abrosimov et al (US PGPub No. 20030097541) discloses a processing architecture for performing a plurality of tasks compises a conveyor of pipe stages, having a certain width and a clock signal.

Wich (US Patent No. 7,071,748) discloses a charge pump clock for a memory device.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

17. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

7-18-06

Mano Padmanabhan 7/20/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER